4 x 37.5 µm Ultra Low Noise InP pHEMT

4F37.5 XX0000

S1
Drain
Gate
S2

45
65
40
60
40
65
20

20 60 117.5 60 20

100
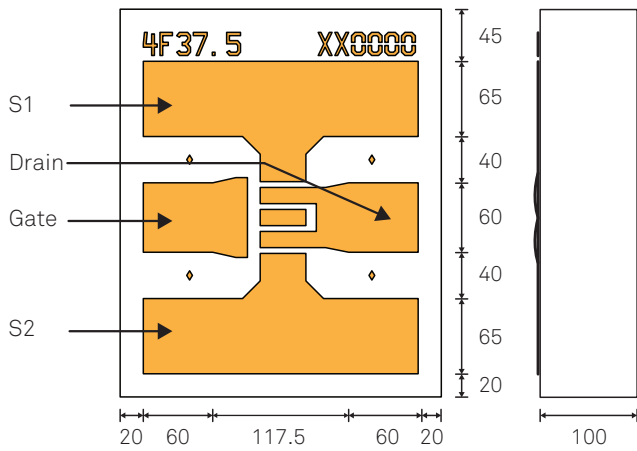
Smaller and larger bond pads are possible on request.
All dimensions are in micrometer.

Basic Characteristics

Temperature	300 K
Transconductance gm	1250 mS/mm
Maximum Drain Current I_{DSmax}	800 mA/mm
Noise Figure NF_{min} (@4 GHz)	0.12 dB
Noise Temperature T_{min} (@4 GHz)	8 K
Associated Gain (@4 GHz)	18.7 dB
Noise Figure NF_{min} (@30 GHz)	0.78 dB
Noise Temperature T_{min} (@30 GHz)	57 K
Associated Gain (@30 GHz)	9.3 dB

Typical Bias Range

V_{DS} = 0.2 V ... 0.75 V

I_{DS} = 20 mA/mm ... 400 mA/mm
    (3 mA ... 60 mA)

V_{GS} = -0.2 V ... 0.25 V

Maximum Ratings

V_{DS} = 1.5 V

V_{GD} = -2.5 V ... 0.5 V

V_{GS} = -1.0 V ... 0.9 V

Die Attach Notes

• Maximum die attach temperature is 200 °C

• It is recommended to use conductive epoxy

• Gold bond wires with diameter of ≤ 22 µm are recommended

• Both source pads (S1, S2) need to be grounded

• To prevent damage to the active area in the center of the die avoid contact to this area during handling
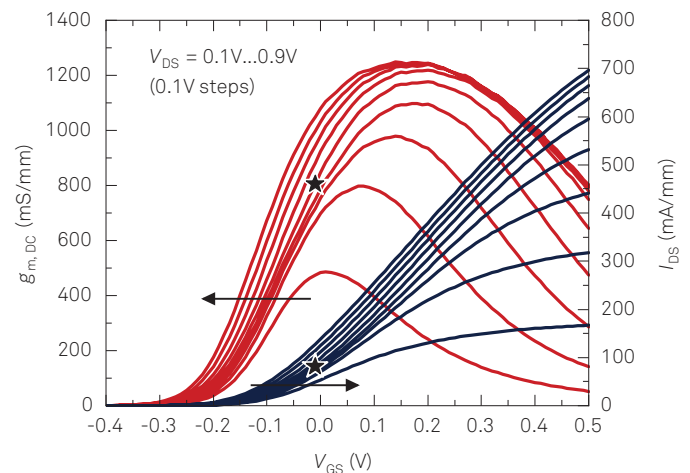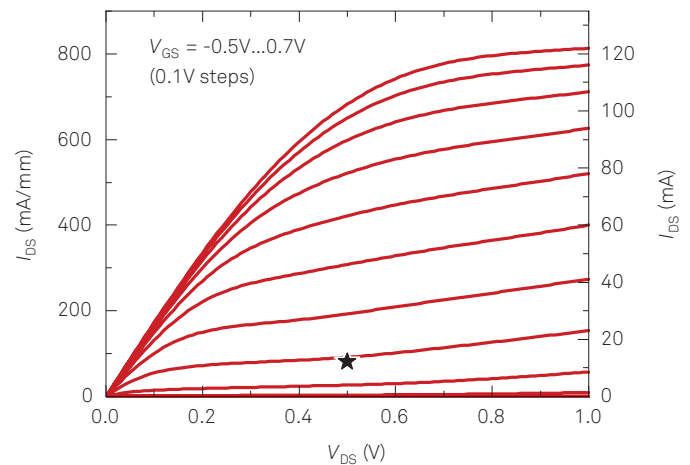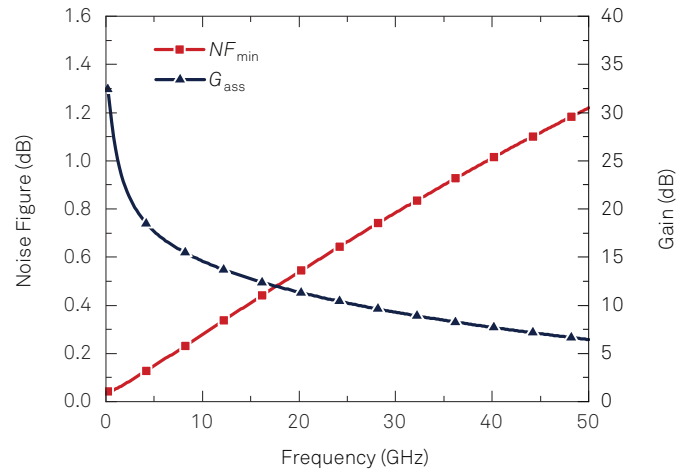
★ *denotes the typical low noise bias point of V_{DS}= 0.5 V and I_{DS} = 80mA/mm (12 mA). The noise figure and gain plot as well as the small-signal model on the back are given for this bias. Data and models for other bias points and operating temperatures are available on request.*

Small-Signal Equivalent Circuit Model
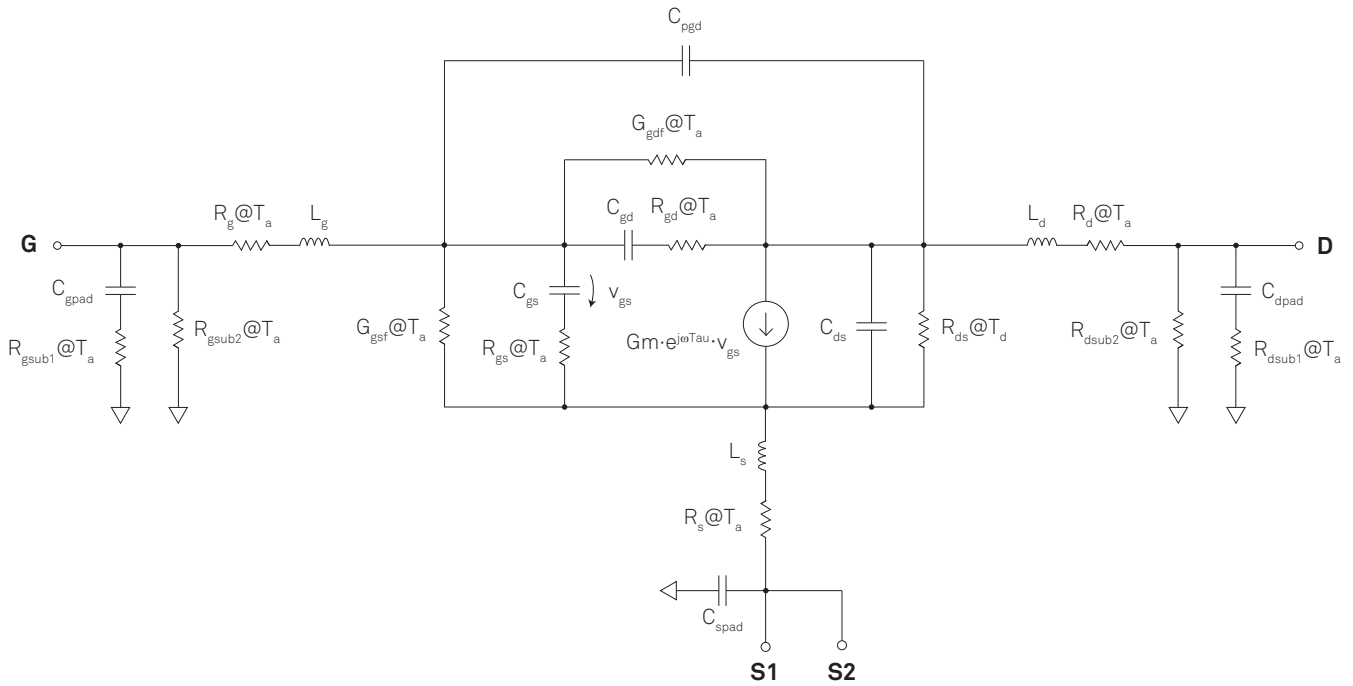
Type	pH-100-4F-37.5
Total Gate Width (µm)	150
Number of Fingers	4
Finger Gate Width (µm)	37.5
Vdrain (V)	0.5
Idrain (mA/mm)	80
Idrain (mA)	12.0
Vgate (V)	~0.00
Ta (K)	300

	Cgpad (fF)	11
	Rgsub1 (Ω)	55
	Rgsub2 (Ω)	0.7M
Pad Parasitics	Cdpad (fF)	11
	Rdsub1 (Ω)	55
	Rdsub2 (Ω)	1.1M
	Cpgd (fF)	2
	Cspad (fF)	84

	Rg (Ω)	0.6
	Rd (Ω)	1.5
	Rs (Ω)	1.4
	Lg (pH)	34
	Ld (pH)	29
	Ls (pH)	5
Chip Equivalent Circuit	Cgs (fF)	102
	Cgd (fF)	42
	Cds (fF)	40
	Rgs (Ω)	1.5
	Rgd (Ω)	2.1
	Rds (Ω)	65
	Ggsf (µS)	0.0
	Ggdf (µS)	1.5
	Gm (mS)	167
	Tau (ps)	0.2
	Td (K)	1703

- For simulation add the bond-wires to the respective ports of the small-signal equivalent circuit (G, D, S1, S2)

- For noise simulation turn on thermal noise in the simulator and set the temperatures to Ta and Td according to the diagram above