multiLane

DATASHEET

Innovation for the next generation

ML407-PAM

Clock Synthesizer for Jitter Tolerance testing | Sinusoidal Jitter Generation| Multi-UI Clock Frequency Modulation

20 MHz to 5.5 GHz Operation | Two Differential Clock Outputs | Low Intrinsic Jitter | FM and PM Modulation |

Summary

With the accelerated growth of hyperscale datacenters, the performance demands on Ethernet network infrastructure is increasing exponentially, and customer expectations for high-speed data throughput is at an all-time high. As a result, Bit Error Rate Testers (BERT) have become a cornerstone for physical layer testing, from qualifying bit transmission for fiber optic and copper-wire digital data transmission lines to testing signal integrity.

A BERT generates a sequence of bits through a communication channel and the received bits are then compared against the transmitted bits. A Bit Error Ratio (BER) evaluates the full end-to-end performance of a connectivity system and assures communication reliability.

The ML407-PAM is an add-on instrument for the MultiLane BERTs, intended for jitter tolerance (JTOL) receiver stress testing. It enables injection of multi-UI sinusoidal jitter, BUJ and random jitter to a clean NRZ or PAM4 signal coming out of the BERT. The ML407-PAM is intended for users seeking to do stressed input testing on their receivers in accordance with OIF-CEI VSR56 PAM or IEEE 802.3 CAUI-4.

ML407-PAM

5.5 GHz Clock Synthesizer

Introduction

The ML407-PAM is an add-on instrument for the ML4039 BERT that can be configured as a clock synthesizer with frequencies ranging from 0.02 to 5.5 GHz

Key Features

- 0.02 to 5.5 GHz operation.
- Two differential clock outputs.
- Low intrinsic jitter
- FM and PM Modulation.

Target Applications

ML4039's clock source for jitter tolerance testing and general serial data receiver characterization.

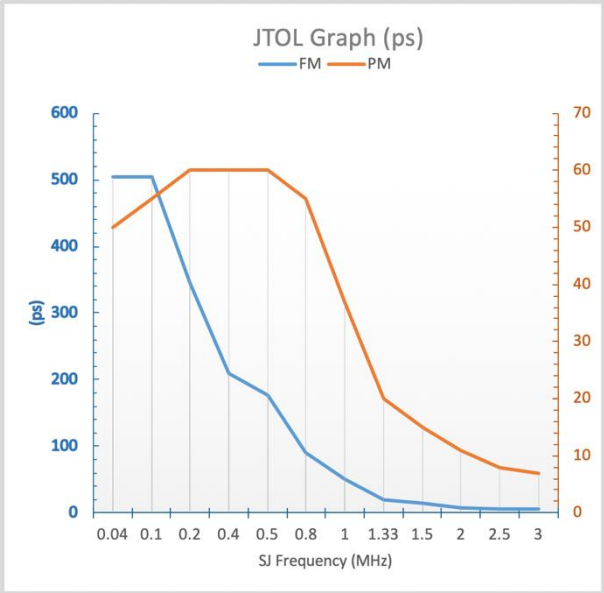
Clock Source

ML407-PAM clock synthesizer generates two pairs of differential clock outputs from 20 MHz to 5.5 GHz.

Setup

ML407 clock out is connected to the clock IN of ML4039D BERT, while the other clock output on the ML407 is terminated with 50 Ω.

JTOL Graph

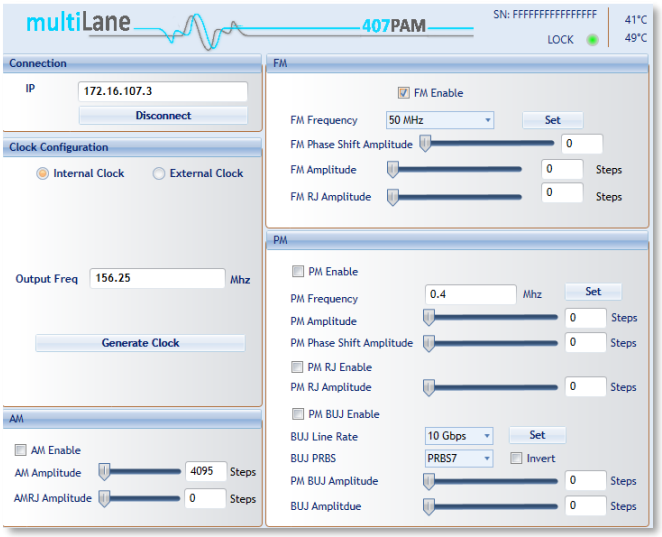


These values were obtained using ML4039D BERT + PX1015D DSO + ML407-PAM Clock Source. The signal is 26.5625 GBd PAM4, and the patterns used are PRBS7 and square wave.

When using the ML407-PAM along with MultiLane BERT instruments, the TX CMU PLL of the driving chip tracks out jitter from its incoming reference CLK at 4 MHz and beyond*, which explains the behavior seen in the JTOL graph. Jitter observed from 4 to 40 MHz is typically out of band noise or crosstalk.

*JTOL SJ jitter impairment from 4 to 40 MHz is not strictly compliant with the stressed receiver sensitivity specification described in the IEEE 802.3bs document, Annex 120D.

Graphical User Interface



The GUI is divided into 5 sections as follows:

Connection

The ML407-PAM has a static IP address and an Ethernet interface that connects to your Windows OS. The very first thing to do in the GUI is to establish a TCP/IP connection to the device.

Clock Configuration

The ML407-PAM has a built-in reference oscillator that is active when “internal clock” radio button is selected.

Range of bit rates	Divider	Example
25 Gbps or GBd	170	For 26.5625 Gbps, use 156.25 MHz clock
50 Gbps or GBd	340	For 53.125 Gbps, use 156.25 MHz clock

FM

FM modulation is the basis for injecting sinusoidal jitter SJ on a PRBS pattern coming out of the BERT. Use the FM controls to do JTOL tests per IEEE or OIF-CEI.

PM

PM stands for phase modulation and is only available on TX2 of the ML407-PAM.
PM modulates the phase of the clock coming out of the ML407-PAM, either in a sinusoidal way, a random way or as BUJ.

Specifications

Synthesizer

Parameter	Specifications
Frequency Range	20 MHz to 5.5 GHZ
Frequency Resolution	1 Hz
TX1 Amplitude Range	1.8 Vpp max
TX2 Amplitude Range	1.8 Vpp max
TX2 Clock Divider	1/2/4/8
External Clock	Single ended or differential input (5 to 1400 MHz)
External Clock Input voltage	0.2 – 2 Vp-p, differential

Electrical

Parameter	Specifications
Power Requirements	12 V 1 A

Mechanical

Parameter	Specifications
TX/RX Connectors	SMA
Box Dimensions (W x L x H)	154 x 161 x 32 mm

Appendix A: Jitter Modulation Examples

These examples use the ML407-PAM clock synthesizer to supply a reference clock to the ML4039D 28GBd PAM4 BERT

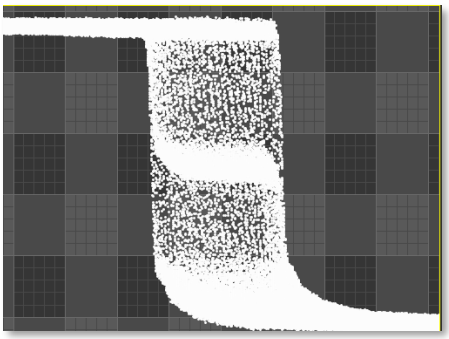


Figure 1: 500 ps SJ Jitter at 40 kHz

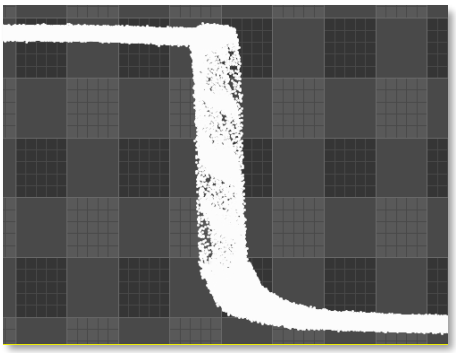


Figure 2: 170 ps SJ Jitter at 0.5 MHz

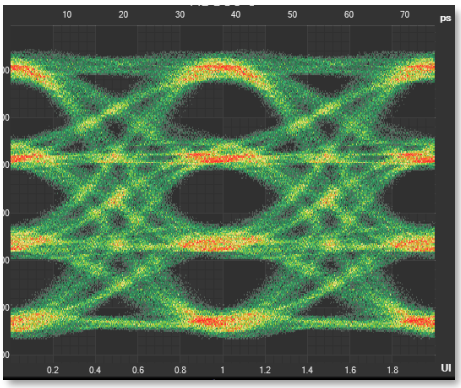


Figure 3: Clean PAM4 eye diagram at 26.5625 GBd

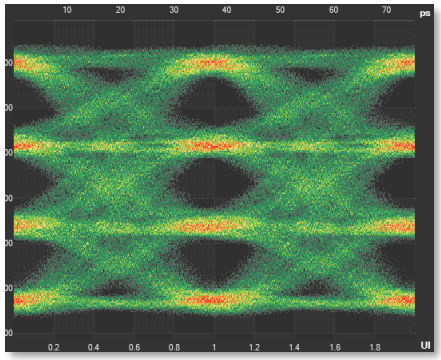


Figure 4: With SJ Jitter at 100 kHz

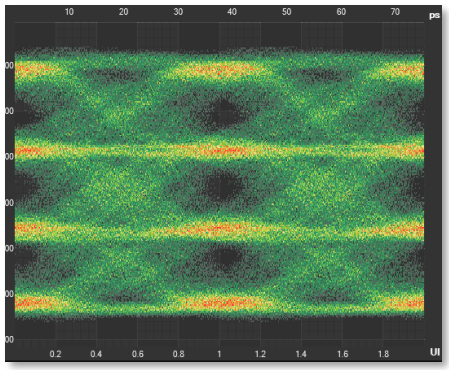


Figure 5: With SJ Jitter at 1 MHz

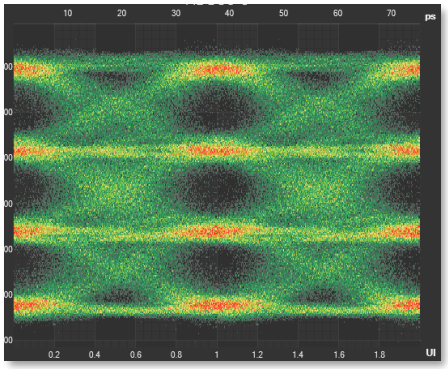


Figure 6: With FM-RJ at 3000 steps (?)

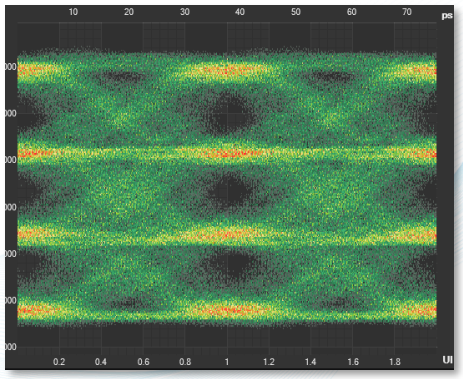


Figure 7: With PM at 0.5 MHz

Ordering Information

Option	Description
ML407-PAM	JTOL Clock Synthesizer 5.5 GHz

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